

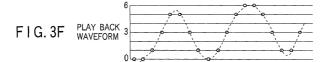
FIG. 2

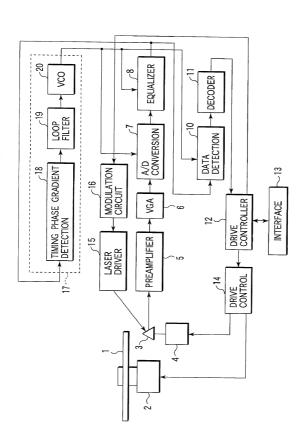




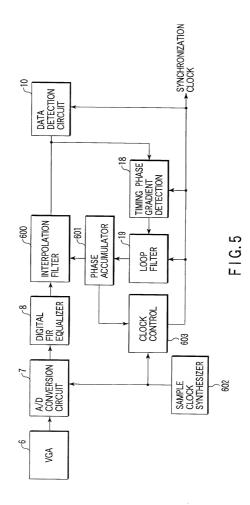
FIG. 3C WRITING 00111100001111100011







F1G.4



F I G. 6

COMPARATOR



FIG.7B WRITING SIGNAL



FIG. 7C WRITING BIT ROW

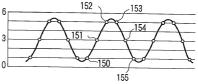
11100011100011100

FIG.7D

FIG. 7E

0 0 1 2 2 1 1 2 2 1 1 2 2 1 1 2 2 1 0 0 1 3 5 5 3 1





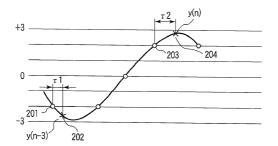


FIG.8A

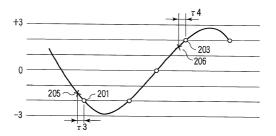


FIG.8B

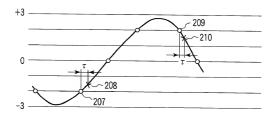


FIG.9A

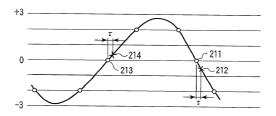


FIG.9B

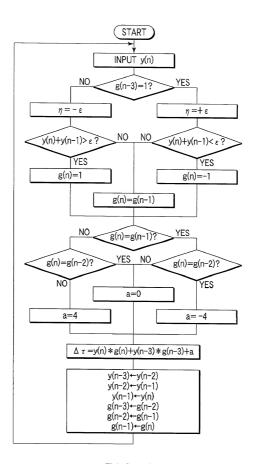
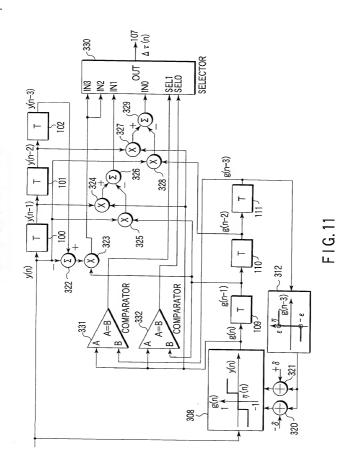
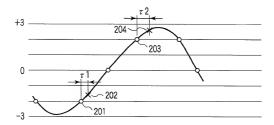


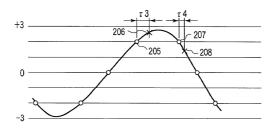
FIG. 10



TOP & HILD TEST



F I G. 12A



F I G. 12B

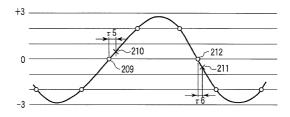


FIG. 13

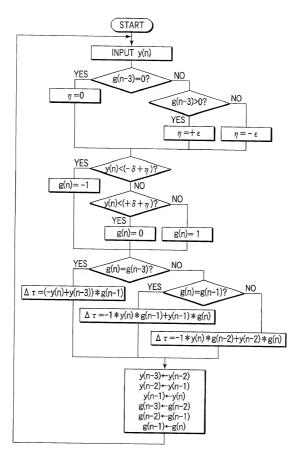
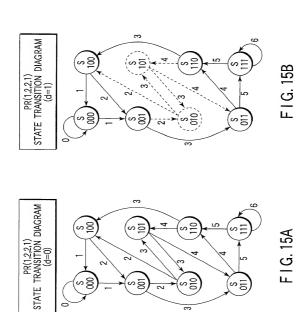


FIG. 14

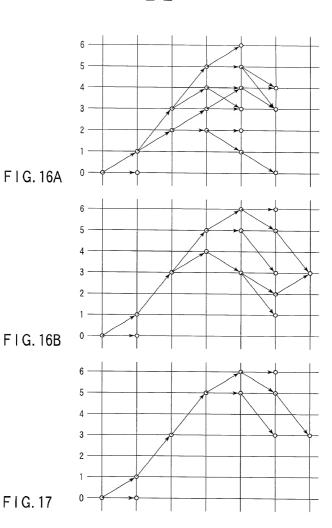
က

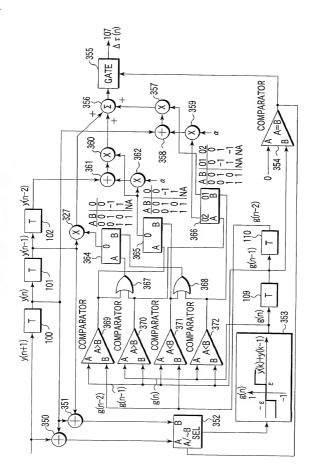
PR(1,2,2,1) TRANSITION DIAGRAM

(d=5)

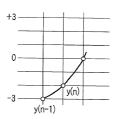


F1G.15C





F1G. 18



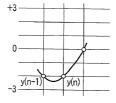
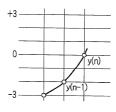


FIG. 19A

F I G. 19B



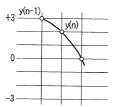
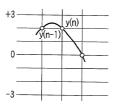


FIG. 19C

FIG. 19D



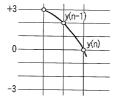
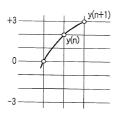


FIG. 19E

FIG. 19F



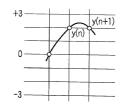
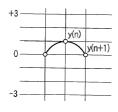


FIG. 20A

FIG. 20B



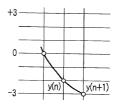
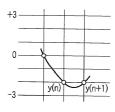


FIG. 20C

FIG. 20D



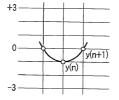
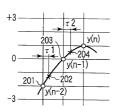
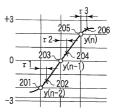


FIG. 20E

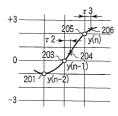
FIG. 20F





F I G. 21A

FIG. 21B



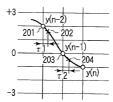
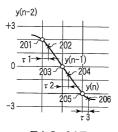


FIG. 21C

FIG. 21D



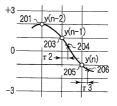
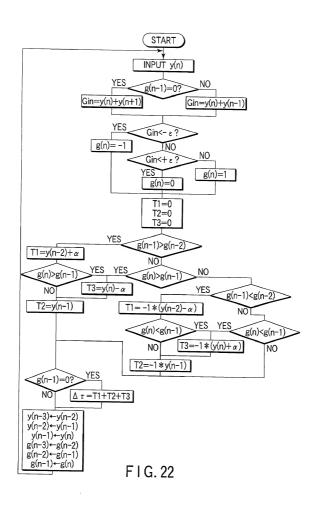


FIG. 21E

F I G. 21F



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F1G.23

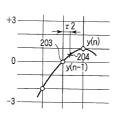
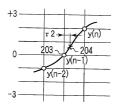


FIG. 24A

F I G. 24B



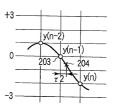
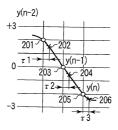


FIG. 24C

FIG. 24D



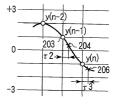


FIG. 24E

FIG. 24F

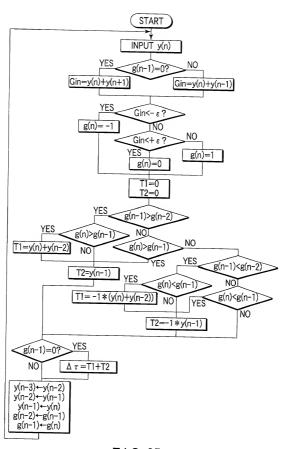


FIG. 25

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Paner and Paner

F1G.26

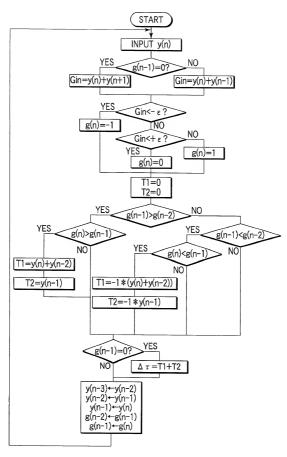


FIG. 27